* K C - 8 0 6 5 *

KC-8065

B. E. II (Sem. III) (ECC) Examination

November / December – 2012

Digital Logic Design

(New Syllabus)

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. II (SEM. III) (ECC)

Name of the Subject :

☛ DIGITAL LOGIC DESIGN (NEW SYLLABUS)

☛ Subject Code No. : 8 0 6 5 ☛ Section No. (1, 2,.....) : Nil

Seat No. :

Student's Signature

(2) All questions are compulsory.

(3) Figures to the right indicate full marks.

(4) Assume necessary data if required.

(5) Justify your answer with proper explanation.

1 (a) Answer following questions : **10**

(1) Convert binary number (1101.1) to its decimal equivalent.

(2) Convert 0.1289062 decimal number to its hex equivalent.

(3) Prove : $A + \overline{A}B + A\overline{B} = A + B$.

(4) Simplify following boolean function :

$$AC + C\left(A + \overline{A}B\right)$$

(5) Draw logic diagram of a half-substractor.

(b) (1) Simplify the expression : **5**

$$Z = AB + A\overline{B} \cdot \left(\overline{\overline{A}\,\overline{C}}\right)$$

(2) Reduce the following function using karnaugh map technique : **5**

$$f(A, B, C, D) = \overline{A}\overline{B}D + AB\overline{C}\overline{D} + \overline{A}BD + ABC\overline{D}$$

2 (a) Implement the following Boolean function with NAND-NAND logic : **8**

$$Y = AC + ABC + \overline{A}BC + AB + D$$

(b) Design a 2-bit comparator using gates. **7**

OR

2 (a) Design a 4-bit binary to gray code converter. **8**

(b) Design a 4-bit parallel adder using full-adders. **7**

3 Write short notes on any three : **15**

(1) Full adder

(2) Priority encoder

(3) Programmable Logic Array (PLA)

(4) Read Only Memory (ROM)

(5) Magnitude comparator.

4 (a) Do as directed : **10**

(1) Give the definition of the propagation delay.

(2) Give the difference between 'Combination Circuit' and 'Sequential Circuit'.

(3) Give block diagram of the sequential circuit.

(4) In J-K flip flop output is _____ when J = 1, K = 1.

(5) Race around problem is solved by _____.

(6) The number of flip-flop required to implement mod-7 counter are _____.

(7) The number of state in ring counter having 4 number of Flip-Flop are _____.

(8) Give the Excitation table for J-K Flip Flop.

(9) Twisted ring counter is also known as _____ counter.

(10) If the clock having frequency 50 Hz is applied to input of the T Flip-Flop, than output clock has frequency of _____.

(b) Attempt the following questions :

(1) Explain serial in serial out shift register. **4**

(2) Design and implement mod-6 asynchronous counter using T flip-flop. **6**

5 (a) Explain Edge Trigger Flip-Flop in detail. **7**

(b) List the type of the shift register and explain bi-direction shift register. **7**

OR

5 (a) What is time race problem ? Explain working of the 'Master-Slave' Flip Flop with timing diagram. **7**

(b) Explain two bit 'ripple up counter', two bit 'ripple down counter' and two bit 'ripple up/down counter', with timing diagram. **7**

6 Attempt any **two** : **16**

(a) Explain shift register counter with timing diagram.

(b) Write down applications of Flip-Flop in detail.

(c) Write short note characteristics of Logic Families.